UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,444	09/29/2003	Ling Ma	IR-2238 (2-3706)	4132

7590 08/19/2004

OSTROLENK, FABER, GERB & SOFFEN
1180 Avenue of the Americas
New York, NY 10036-8403

EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,444	MA ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 13-20* is/are rejected.

7)☒ Claim(s) *3-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 2 and 13-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsui U.S. Patent 6,489,204 B1.

5. Tsui discloses a semiconductor process as claimed. See **FIGS. 1A-9**, where Tsui teaches the claimed invention.

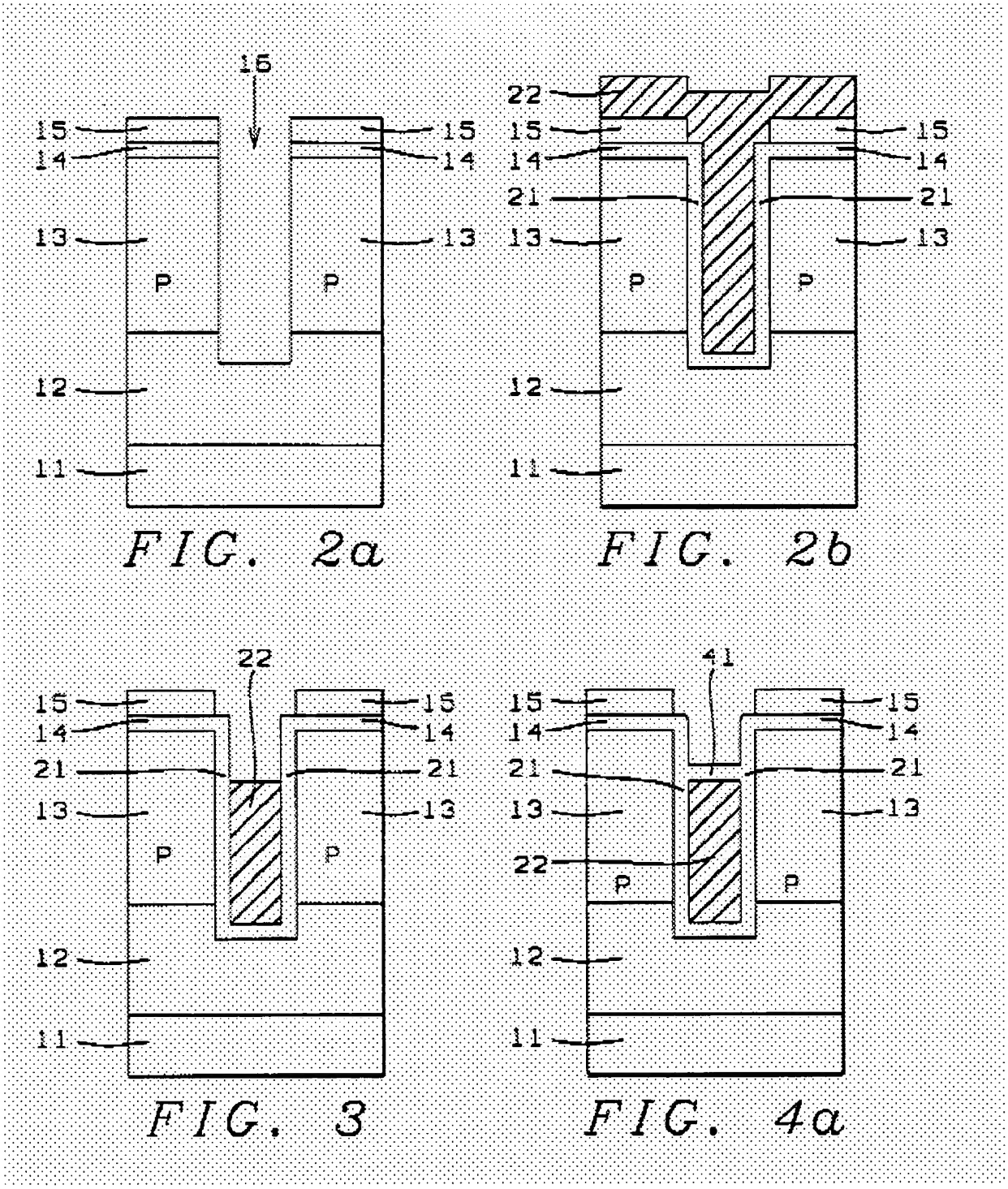


FIG. 2a FIG. 2b

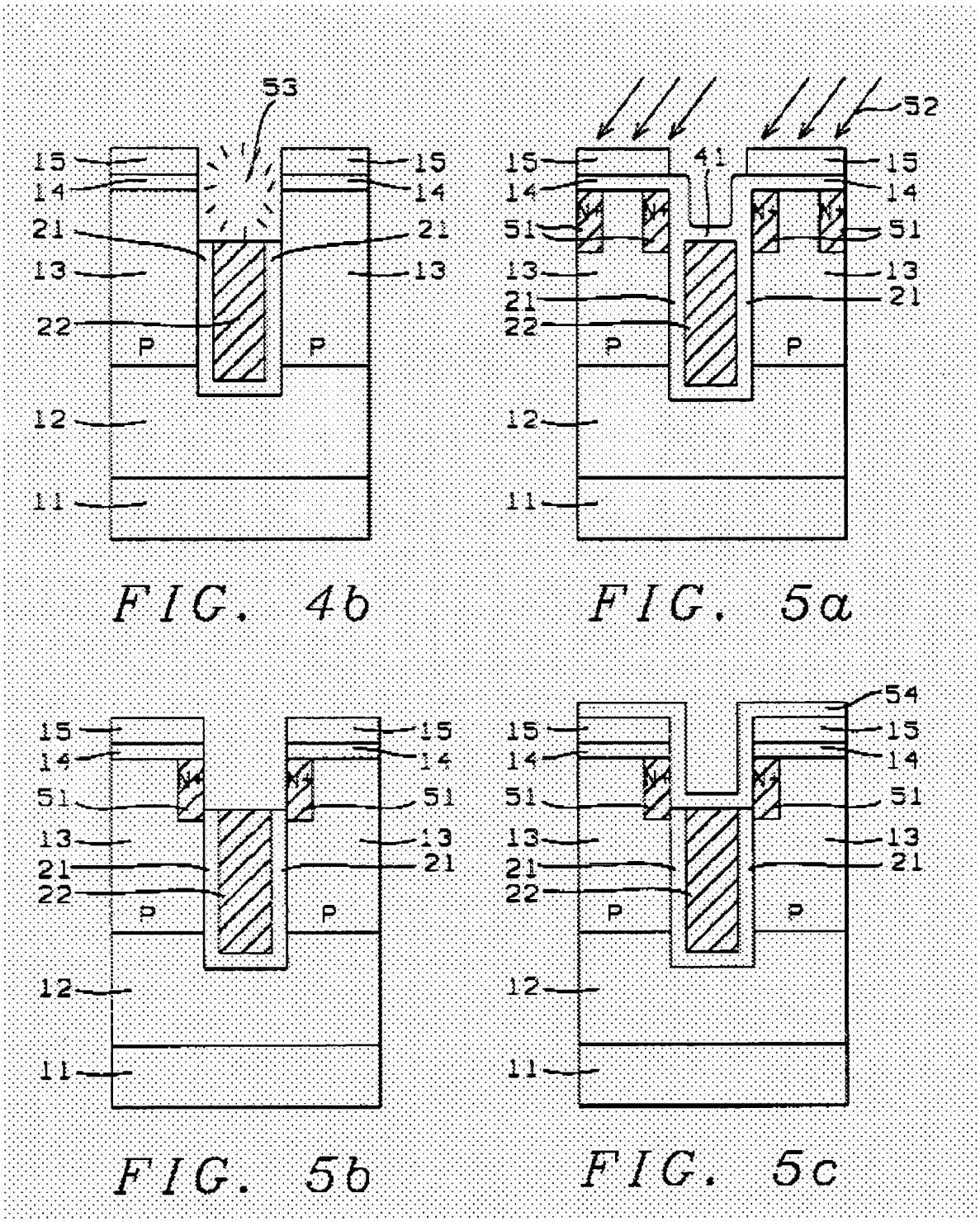
FIG. 3 FIG. 4a

6. Pertaining to claim 1, Tsui teaches a method for manufacturing a semiconductor device comprising:

providing a semiconductor die (not numbered) of a semiconductive material having a channel receiving layer **13** of a first conductivity;

forming a layer of oxidation retardant material **15**, (i.e., silicon nitride)over said channel receiving layer;

forming trenches **16** in said channel receiving layer in one region of said channel receiving layer;



forming a termination recess (the area above **21**) around said trenches said termination recess having exposed surfaces of semiconductive material **13**;

forming another layer of oxidation retardant material over sidewalls and bottom of each of said trenches; and

growing an oxide layer **54** on exposed surfaces of said termination recess.

7. Pertaining to claim 2, Tsui teaches a method according to claim 1, further comprising implanting channel dopants of a second conductivity in said channel receiving layer before forming said layer of oxidation retardant material; and

diffusing said channel dopants after forming said layer of oxidation retardant material to form a channel region (as seen in **FIG. 1d**).

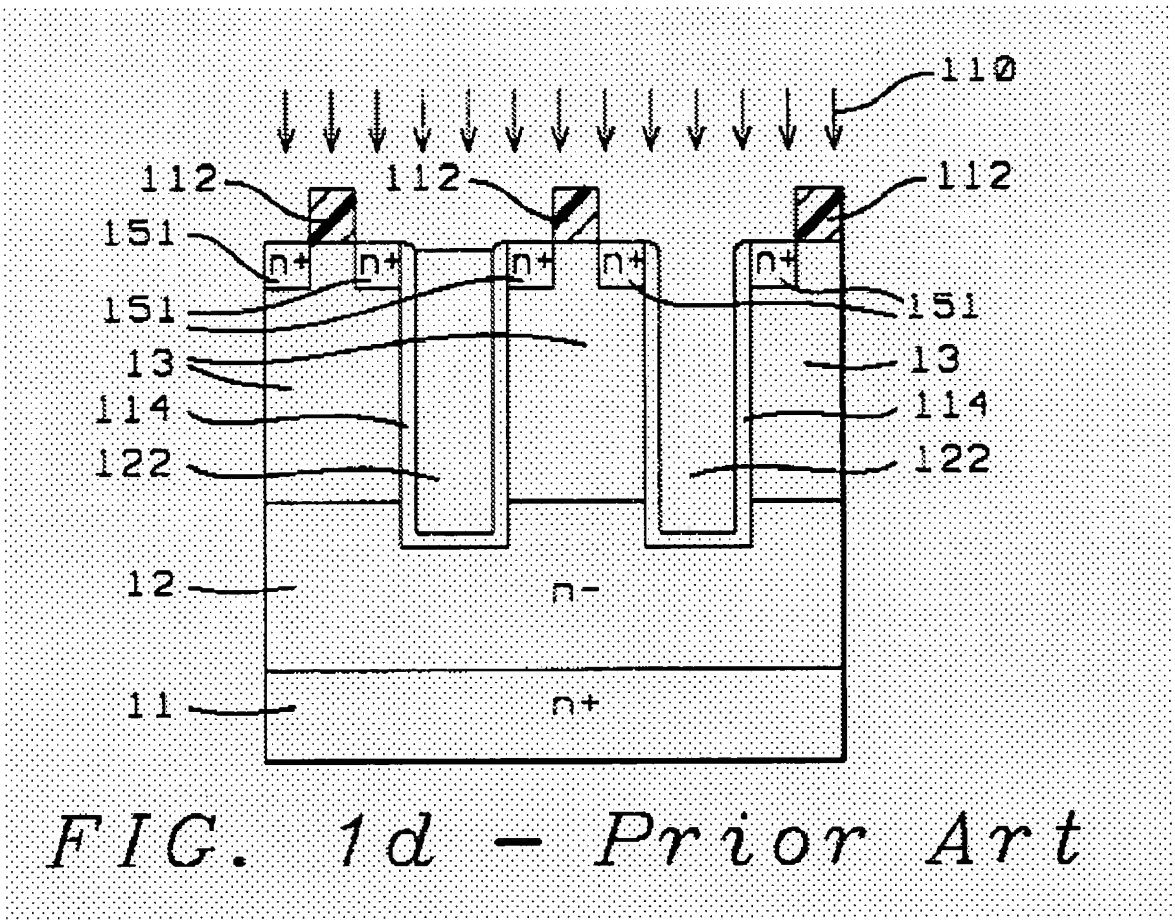


FIG. 1d – Prior Art

8. Pertaining to claim 13, Tsui teaches a method according to claim 1, wherein said oxidation retardant material is a nitride.

9. Pertaining to claim 14, Tsui teaches a method according to claim 1, wherein said channel receiving layer is an epitaxial layer of first conductivity formed over a monolithic substrate of said first conductivity (please see column 1, lines 17-19).

10. Pertaining to claim 15, Tsui teaches a method according to claim 1, wherein said semiconductor device is a MOSFET.

11. Pertaining to claim 16, Tsui teaches a method for manufacturing a MOS-gated semiconductor switching device, comprising:

providing a semiconductor die (not numbered) having a channel receiving region of first conductivity **12**;

forming a channel region of second conductivity **13** in said channel receiving region (the Examiner takes the position that there are only two type of conductivities in MOS-gated semiconductor devices and both conductivities are required for a functional device);

forming at least one trench **16** in said semiconductor die extending through said channel region **13**;

forming a gate structure **22** in said at least one trench; and

forming a conductive region **51** of said first conductivity type adjacent each side of said trench in said channel region after forming said gate structure.

12. Pertaining to claim 17, Tsui teaches a method according to claim 16, wherein said forming said conductive region comprises implanting dopants of said first conductivity in said channel region;

applying a contact mask (see **FIG. 5a**, above) for forming a metal contact (**101** of **FIG. 1e**) over said semiconductor die to serve as external connection for said conductive region;

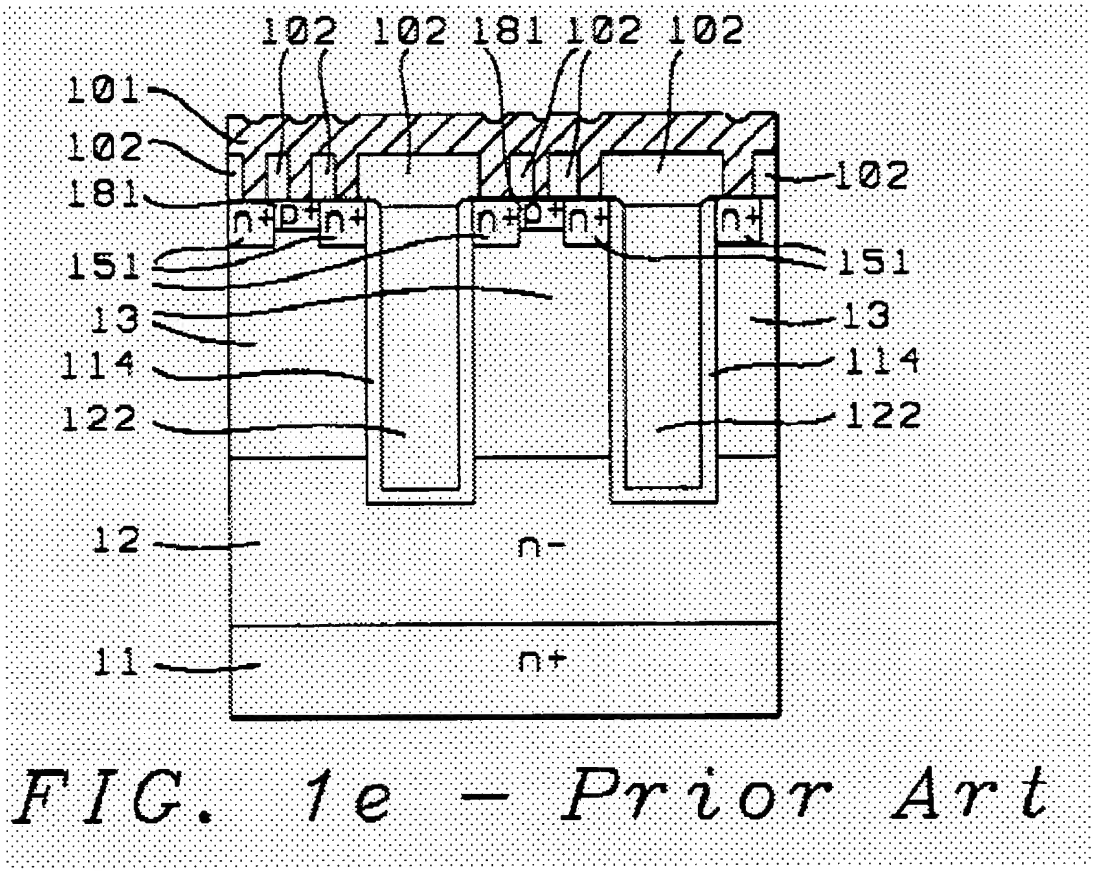


FIG. 1e – Prior Art

etching a depression through said conductive region to reach said channel region using said mask;

implanting dopants of said second conductivity at the bottom of said depression, and diffusing said dopants of said first conductivity in a diffusion drive to form said conductive regions.

13. Pertaining to claim 18, Tsui teaches a method according to claim 16, further comprising forming a layer of oxidation retardant material on said sidewalls of said at least one trench, and forming a thick oxide at the bottom of said trench (the Examiner takes the position that the term "thick" is a relative term and allows for any material having a dimension to meet this limitation).

14. Pertaining to claim 19, Tsui teaches a method according to claim 16, further comprising forming a termination structure in said semiconductor die, said termination structure including a recess formed in said semiconductor die.

15. Pertaining to claim 20, Tsui teaches a method according to claim 16, wherein said gate structure includes a gate electrode **22** insulated from said trench sidewalls by an insulation layer **21**, wherein said insulation layer is formed by thermal oxidation before forming said conductive regions.

Objections

16. Claims 3-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC